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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/721,677	11/27/2000	Soren Norskov	367.39268X00	4372

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EXAMINER
ALCALA, JOSE H

ART UNIT	PAPER NUMBER
2827	

DATE MAILED: 10/22/2002

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/721,677	NORSKOV, SOREN	
	Examiner	Art Unit	
	Jose H Alcala	2827	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *21 December 2001* .

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *22-49* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *22-49* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *27 November 2000* is/are: a)☐ accepted or b)☒ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☒ The proposed drawing correction filed on *21 December 2001* is: a)☒ approved b)☐ disapproved by the Examiner

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449) Paper No(s) *8* .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: .

DETAILED ACTION

1. This final rejection is in response to amendment filed on 12/21/01.

Drawings

2. The proposed drawing correction and/or the proposed substitute sheets of drawings, filed on 12/21/01 have been approved, however there are some other objections pointed out below. A proper drawing correction or corrected drawings are required in reply to the Office action to avoid abandonment of the application. The correction to the drawings will not be held in abeyance.

3. Figure 1 is improperly crosshatched. All of the parts shown in the section, and only those parts, must be crosshatched. For example the conductive path, and the vias need to be changed to have the correct crosshatching showing that the material of those elements is conductive. In addition, the elements that are made of a dielectric material, need to be identified with the proper crosshatching as pointed in the MPEP section below. The crosshatching patterns should be selected from those shown on page 600-81 of the MPEP based on the material of the part. See also 37 CFR 1.84(h)(3) and MPEP 608.02.

The drawings are objected to under 37 CFR 1.83(a). The drawings must show every feature of the invention specified in the claims. Therefore, the first capacitor plate needs to be shown to be provided within the chip, as recited in Claim 1. Furthermore, the via needs to be shown to be: "electrically coupled in series with the second

capacitor plane". In addition, the dielectric layer being an integral part of the chip, as recited in claims 24 and 25. Additionally the "layer of conductive glue", needs to be shown provided between the metallic layer and the dielectric layer, as recited in claims 38-45. These elements must be shown or the feature(s) canceled from the claim(s). No new matter should be entered.

A proposed drawing correction or corrected drawings are required in reply to the Office action to avoid abandonment of the application. The objection to the drawings will not be held in abeyance.

Claim Objections

4. Applicant is advised that should claim 24 be found allowable, claim 25 will be objected to under 37 CFR 1.75 as being a substantial duplicate thereof. In addition, should claim 26 be found allowable, claim 27 will be objected. Should claim 28 be found allowable, claim 29 will be objected. Should claim 30 be found allowable, claims 31-37 will be objected. Should claim 38 be found allowable, claims 39-45 will be objected. When two claims in an application are duplicates or else are so close in content that they both cover the same thing, despite a slight difference in wording, it is proper after allowing one claim to object to the other as being a substantial duplicate of the allowed claim. See MPEP § 706.03(k).

Claim Rejections - 35 USC § 112

5. The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

6. Claims 22-47 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

Claim 22 is unclear in the first two lines, regarding the scope of the invention. It is unclear if the claimed invention is the ground plane, and the recitation: "for mounting on a supporting member in a chip package", is merely an intended use limitation. In addition it is unclear if the invention is directed to the supporting member or to the chip package. The invention as claimed is not positively reciting the "supporting member" and the "chip package", thus whenever those elements are mentioned later in the claim they are treated as not having antecedent basis. In addition, line 2 is unclear regarding what is labeled as the "supporting member". Furthermore, it is not clear what element or elements are part of that "supporting member", both in the drawings and in the specification. In addition it is further unclear how can the ground plane comprise a "first conductive member" and include the "at least one electrically conductive via", at the same time. It is unclear how can the via be: "electrically coupled in series with the second capacitor plane", if the via is not located near the second capacitor plane according to specification and drawings. It is further unclear how can the "second capacitor plate" in line 9, comprise a layer of conductive glue.

Claim 23 is claiming a function of the device, but is not claiming the structural element that is responsible for that function. For examining purposes, this claim fails to further limit the invention structurally.

Claims 24 and 25 are not clear regarding how can the dielectric layer be an integral part of the chip. For examining purposes, it is assumed to mean that the dielectric layer is an integral part of the **chip package.**

Claims 26 and 27 are not clear regarding how can the dielectric layer be an integral part of the chip and at the same time cover an entire surface of the chip. For examining purposes, it is assumed to mean that the dielectric layer has the same width as the supporting member.

Regarding claims 28 and 29 it is unclear how can a "**dielectric layer**" comprise "silicon oxide", if "silicon oxide" is a **semiconductor**. While applicant may be his or her own lexicographer, a term in a claim may not be given a meaning repugnant to the usual meaning of that term. See *In re Hill*, 161 F.2d 367, 73 USPQ 482 (CCPA 1947). The term "dielectric" in claims 28 and 29 is used by the claim to mean "semiconductor," while the accepted meaning is "a nonconductor of direct electrical current." For examination purposes it is impossible to have a dielectric layer made of silicon oxide, therefore the limitation is not considered.

Claims 30-37 are not clear regarding how can the second capacitor plate be a metallic layer and a conductive glue at the same time, or if the plate is composed of both materials, or if instead of having a single capacitor plate there is a second capacitor element comprising two plates.

Claims 38-45 are unclear regarding how is the layer of conductive glue located regarding to the other elements of the invention, such as the first capacitor plate.

Claim 48 is unclear in the first two lines, regarding the scope of the invention. It is unclear if the claimed invention is a method for making a ground plane, or a method of making a chip package.

Claim Rejections - 35 USC § 103

7. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

8. Claim 22-48 are rejected under 35 U.S.C. 103(a) as being unpatentable over Blaupunkt (EP 0630176 A1) in view of Selna (US Patent No. 5,741,729). As best understood by the examiner:

Regarding Claim 22, Blaupunkt teaches at least one first capacitor plate (Reference numbers 2 and 3), and at least one second capacitor plate (Reference number 5), the first and second capacitor plates being separated by a dielectric layer (Reference number 6) and capacitively coupled to each other via the dielectric layer, and wherein the first comprises a layer of conductive glue.

Blaupunkt fails to teach a ground plane for a semiconductor chip for mounting on a supporting member in a chip package, and the ground plane comprising at least one first conducting member, including at least one electrically conducting via.

Selna teaches a ground plane (Reference number 60) for a semiconductor chip for mounting on a supporting member in a chip package, and the ground plane (Reference number 60) comprising at least one first conducting member (The layer of Reference number 60), including at least one electrically conducting via (Reference number 6c).

It would have been obvious to one of ordinary skill in the art at the time the invention was made to combine the teachings of Selna and Blaupunkt in order to have the invention of Blaupunkt to be attached to the support structure having the ground layer as taught by Selna, thus helping maintain the current flow in the package and reducing ground bounce and reducing IC signal delay time.

Regarding Claim 23, Blaupunkt as modified by Selna teaches all the structural elements of claim 22, thus it is inherent that the structure has a resonant frequency of the capacitance provided by the first capacitor plate and the second capacitor plate, and an inductance provided by the at least one first conducting member, is approximately equal to an intended working frequency of the chip.

Regarding Claims 24 and 25, Blaupunkt as modified by Selna teaches that the dielectric layer is an integral part of the **chip package**.

Regarding claims 26 and 27, it would have been obvious to one of ordinary art at the time of the invention to further modify the combination of Blaupunkt and Selna, in order to make the dielectric layer covering an entire surface of the supporting member, in order to make the two elements having the same width, improving integration and

making the package compact and lightweight by reducing the material used for the supporting member.

Regarding Claims 28 and 29, Blaupunkt as modified by Selna teaches a dielectric layer (Blaupunkt reference number 6).

Regarding Claims 30-37, Blaupunkt as modified by Selna teaches that the second capacitor plate (Blaupunkt reference number 5) is a metallic layer on the supporting member.

Regarding Claims 38-45, Blaupunkt as modified by Selna fails to explicitly teach that the layer of conductive glue is provided between the metallic layer and the dielectric layer. It would have been obvious to one of ordinary skill in the art at the time the invention was made to make the layer of conductive glue provided between the metallic layer and the dielectric layer, since it has been held that rearranging parts of an invention involves only routine skill in the art. In re Japikse, 86 USPQ 70.

Regarding Claim 46, Blaupunkt as modified by Selna, fails to explicitly teach that the at least one electrically conducting via extending through the supporting member is directly connected to the second capacitor plate improving integration and making the package compact and lightweight by reducing the material used for the supporting member. It would have been obvious to one of ordinary skill in the art at the time the invention was made to make the electrically conducting via to be directly in contact with the second capacitor plane in order to improve integration and thus helping maintain the current flow in the package and reducing ground bounce and reducing IC signal delay time.

Regarding Claim 47, the limitation that the vias and the metallic layer are integrally formed from a same metal, is a product by process limitation. If the product in the product-by-process claims are the same as or obvious from a product of the prior art, the claims are unpatentable even tough the prior product was made by a different process. See In re Thorpe, 227 USPQ 964,966 (Fed.Cir 1985). A "product by process" claim is directed to the product per se, no matter how actually made, In re Brown, 173 USPQ 685; In re Luck, 177 USPQ 523; In re Fessmann, 180 USPQ 324; In re Avery, 186 USPQ 161; In re Wertheim, 191 USPQ 90 (209 USPQ 554 does not deal with this issue); In re Marosi et al, 218 USPQ 289; and particularly In re Thorpe, 227 USPQ 964, all of which make it clear that it is the patentability of the final product per se which must be determined in a "product by process" claim, and not the patentability of the process, and that an old or obvious product produced by a new method is not patentable as a product, whether claimed in "product by process" claims or not. Note that applicant has the burden of proof in such cases, as the above case law makes clear.

Regarding Claim 48, Blaupunkt inherently teaches a method for providing a semiconductor chip (Reference number1) mounted on a supporting member in a chip package, comprising providing a metal covered area (reference number 3) on the surface of the supporting member, providing vias (Reference number 4) electrically connected to the metal covered area and extending there from through the supporting member to the opposite side thereof, connecting in parallel at least two of the vias, and using a conductive glue (Reference number 2) between the chip and the metal covered

area to attach the metal covered area to the chip. Blaupunkt fails to teach a ground plane for a semiconductor chip for mounting on a supporting member in a chip package.

Selna teaches a method of making a ground plane (Reference number 60) for a semiconductor chip for mounting on a supporting member in a chip package.

It would have been obvious to one of ordinary skill in the art at the time the invention was made to combine the teachings of Selna and Blaupunkt in order to have the method of making the invention of Blaupunkt to be attached to the support structure having the ground layer as taught by Selna, thus helping maintain the current flow in the package and reducing ground bounce and reducing IC signal delay time.

9. Claim 49 is rejected under 35 U.S.C. 103(a) as being unpatentable over Blaupunkt (EP 0630176 A1) in view of Jedlicka et al. (US Patent No. 4,954,197). As best understood by the examiner:

Regarding Claim 49, Blaupunkt teaches a semiconductor chip package comprising: a semiconductor chip (Reference number 1) and a supporting member, the supporting member comprising at least one metal covered area (Reference number 3) and at least one electrically conductive via (Reference number 4) extending from the metal covered area through the supporting member, wherein the chip is adhered to the supporting member by means of a conductive glue (Reference number 2), but fails to explicitly teach that the conductive glue is in electrical contact with the metal covered area.

Jedlicka teaches a chip (Reference number 5), a conductive glue (Reference number 20) in electrical contact with the metal covered area (Reference number 8).

It would have been obvious to one of ordinary skill in the art at the time the invention was made to combine the teachings of Blaupunkt and Jedlicka in order to have a conductive glue in electrical contact with the metal covered area, thus improving the process of bonding small chips to a substrate and reducing the costs usually involved in the attachment of chips to boards.

Response to Arguments

10. Applicant's arguments filed on 12/21/01 regarding the Blaupunkt (EP 0630176 A1) reference have been fully considered but they are not persuasive.

11. Regarding the argument that EP 630,176 does not disclose: "a conductive glue" but rather a: "thermally conductive glue". It is pointed out that reference number 2 is disclosing a **conductive** glue, and independent claims 22 and 48 recite: "a layer of **conductive** glue", thus the claimed invention does not distinguishes over the prior art.

12. Applicant's arguments with respect to claims 1-21, and regarding references US Patent 4,736,521 and GB 2118371 have been considered but are moot in view of the new ground(s) of rejection.

Conclusion

13. Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

14. A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

15. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure. The following references either teach some of the elements of the instant claimed invention and/or some arrangement of those sections: Hale et al. (US Patent No. 6,407,929 B1), Smith (US Patent No. 5,475,317), Malladi (US Patent No. 5,939,782), Figueroa et al. (US Patent No. 6,388,207 B1), Kakimoto et al. (US Patent No. 6,181,278), Herandez et al. (US Patent No. 5,309,324), Davidson (US Patent No. 6,400,576 B1) and Kelly et al. (US Patent No. 5,798,567).

16. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Jose H Alcala whose telephone number is (703) 305-9844. The examiner can normally be reached on Monday to Friday.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, David Talbott can be reached on (703) 305-9883. The fax phone numbers for the organization where this application or proceeding is assigned are (703) 305-3431 for regular communications and (703) 305-3431 for After Final communications.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is (703) 308-0956.

JHA
October 17, 2002

Albert W. Paladini 10-16-02
ALBERT W. PALADINI
PRIMARY EXAMINER